Instruction Manual

Tektronix

P6960 and P6980
High Density Logic Analyzer Probes
with D-Max™ Probing Technology

071-1528-00

There are no current European directives that apply to this product. This product provides cable and test lead connections to a test object of electronic measuring and test equipment.

Warning
The servicing instructions are for use by qualified personnel only. To avoid personal injury, do not perform any servicing unless you are qualified to do so. Refer to all safety summaries prior to performing service.

www.tektronix.com

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WARRANTY

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In order to obtain service under this warranty, Customer must notify Tektronix of the defect before the expiration of the warranty period and make suitable arrangements for the performance of service. Customer shall be responsible for packaging and shipping the defective product to the service center designated by Tektronix, with shipping charges prepaid. Tektronix shall pay for the return of the product to Customer if the shipment is to a location within the country in which the Tektronix service center is located. Customer shall be responsible for paying all shipping charges, duties, taxes, and any other charges for products returned to any other locations.

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Table of Contents

List of Figures

General Safety Summary

Review the following safety precautions to avoid injury and prevent damage to this product or any products connected to it. To avoid potential hazards, use this product only as specified.

Only qualified personnel should perform service procedures.

While using this product, you may need to access other parts of the system. Read the *General Safety Summary* in other system manuals for warnings and cautions related to operating the system.

To Avoid Fire or Personal Injury

Connect and Disconnect Properly. Connect the probe output to the measurement instrument before connecting the probe to the circuit under test. Disconnect the probe input and the probe ground from the circuit under test before disconnecting the probe from the measurement instrument.

Observe All Terminal Ratings. To avoid fire or shock hazard, observe all ratings and markings on the product. Consult the product manual for further ratings information before making connections to the product.

Do not apply a potential to any terminal, including the common terminal, that exceeds the maximum rating of that terminal.

Avoid Exposed Circuitry. Do not touch exposed connections and components when power is present.

Do Not Operate With Suspected Failures. If you suspect there is damage to this product, have it inspected by qualified service personnel.

Do Not Operate in Wet/Damp Conditions.

Do Not Operate in an Explosive Atmosphere.

Keep Product Surfaces Clean and Dry.

Provide Proper Ventilation. Refer to the manual's instructions for details on installing the product so it has proper ventilation.

Symbols and Terms

Terms in this Manual. These terms may appear in this manual:

WARNING. *Warning statements identify conditions or practices that could result in injury or loss of life.*

CAUTION. *Caution statements identify conditions or practices that could result in damage to this product or other property.*

Terms on the Product. These terms may appear on the product:

DANGER indicates an injury hazard immediately accessible as you read the marking.

WARNING indicates an injury hazard not immediately accessible as you read the marking.

CAUTION indicates a hazard to property including the product.

Symbols on the Product. The following symbols may appear on the product:

Preface

This document provides information on using and servicing the P69xx series logic analyzer probes.

Related Documentation

In addition to these probe instructions, the following documentation is available for your Tektronix 700 Series Logic Analyzers:

- The *Tektronix Logic Analyzer Family User Manual* provides overall user information for the TLA Series Logic Analyzer.
- The *TLA700 Series Logic Analyzer Installation Manual* provides installation information for the TLA700 Series Logic Analyzer.
- The *TLA5000 Series Logic Analyzer Installation Manual* provides installation information for the TLA5000 Series Logic Analyzer.
- The *TLA7Axx/TLA7NAx Module Service Manual* that provides module-level service information for major components of the TLA Series Logic Analyzer.
- *P6810 General Purpose Logic Analyzer Probe Label Instructions*
- *P6860 High Density Logic Analyzer Probe Label Instructions*
- *P6864 High Density 4X Logic Analyzer Probe Label Instructions*
- *P6880 High Density Differential Logic Analyzer Probe Label Instructions*
- *P6960 High Density Logic Analyzer Probe Labeling and Installation Instructions*
- *P6980 High Density Differential Logic Analyzer Probe Labeling and Installation Instructions*
- The online help provides information about the user interface, the TLA700 Programmatic Interface (TPI), and the TLAScript interface. To view the online help, select Help Topics from the Help menu. The TLAScript online help provides links to related topics in TPI.
- The online release notes provide last-minute product and software information not included in this manual. To access the Probe Manual Release Notes, click Start > Programs > Tektronix Logic Analyzer > TLA Release Notes.
- A series of microprocessor support instruction manuals provide operating and service instructions for the individual microprocessor support packages.

- The *TLA7QS QuickStart Training Manual* provides training exercises to help you learn key features of the logic analyzer. The training manual is designed to be used with the TLA7QS QuickStart training board.
- The *P6434 Mass Termination Probe Instructions* provides instructions for using the P6434 Probes with older Tektronix logic analyzers.
- The *P6417 & P6418 Logic Analyzer Probes Instructions* provides instructions for using the P6417 and P6418 Probes.
- The *P6419 Logic Analyzer Probe Instructions* provides instructions for using P6419 Probes.

Commonly Used Terms

Refer to the following list of commonly used terms throughout the manual.

cLGA An acronym for compression Land Grid Array, a connector that provides an electrical connection between a PCB and the probe input circuitry.

Compression Footprint A connectorless, solderless contact between your PCB and the P6960 and P6980 Probes. Connection is obtained by applying pressure between your PCB and the probe through a cLGA c-spring.

Differential Input Amplitude Definition For differential signals, the magnitude of the difference voltage $\overline{V}$max-Vmin (and Vmin-$\overline{V}$max) must be greater than or equal to 150 mV. Refer to Figure i.

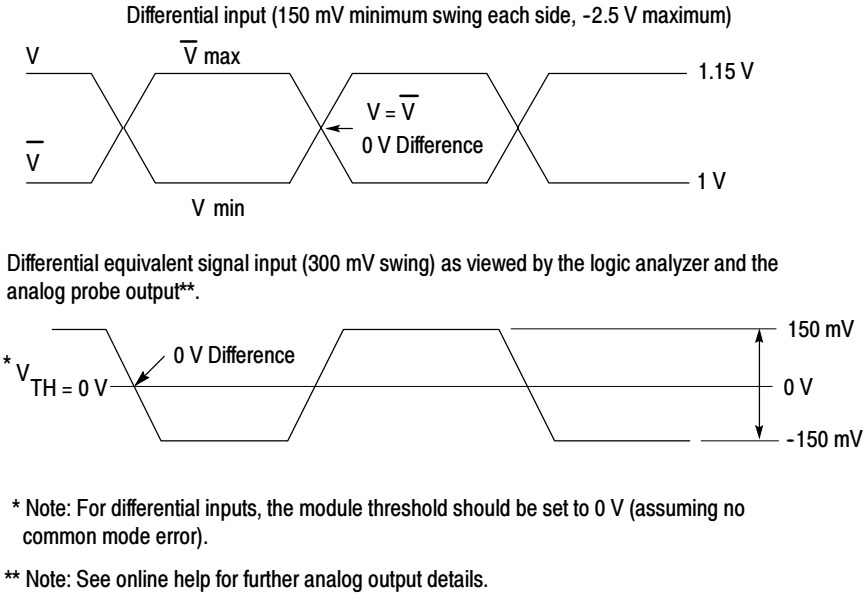

Figure i: Differential input amplitude

D-Max probing technology Trademark name that describes the technology used in the P6960 and P6980 high-density logic analyzer probes.

Flying Lead Set A lead set designed to attach to a P6960 Probe to provide general-purpose probing capability. See Figure ii.

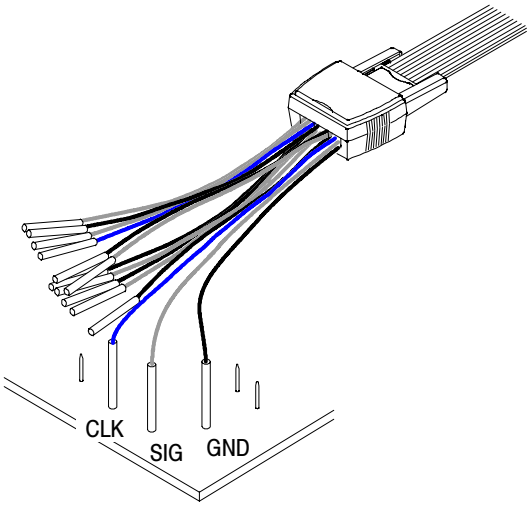

Figure ii: Flying Lead Set

Functional Check Procedure Functional check procedures verify the basic functionality of the probes by confirming that the probes recognize signal activity at the probe tips.

Keepout Area An area on a printed circuit board in which component, trace, and/or via placement may be restricted.

Module The unit that plugs into a mainframe that provides instrument capabilities such as logic analysis.

Module End The end of the probe that plugs into the module unit.

PCB An acronym for Printed Circuit Board; also known as Etched Circuit Board (ECB).

Probe The device that connects a module with a target system. See Figure iii.

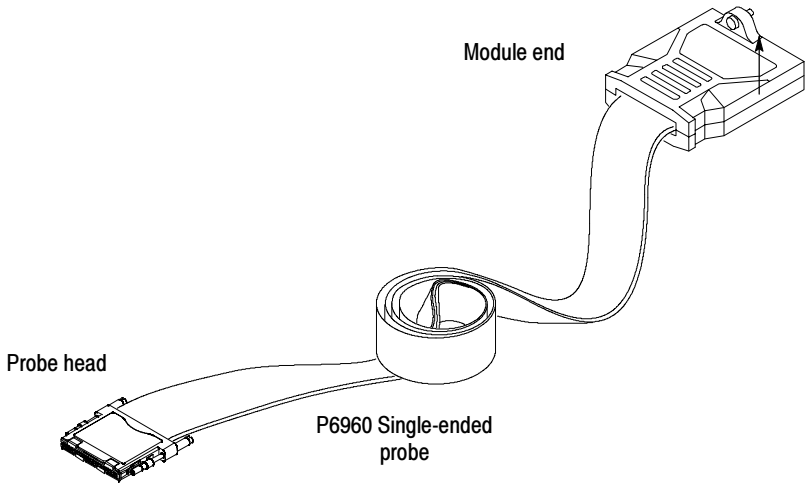

Figure iii: Probe example

Probe Adapter A device that connects the LA module probe to a target system.

Probe Head The end of the probe (see Figure iii) that connects to the target system or probe adapter.

SMT KlipChip An interface device for attaching logic analyzer probes to components with a maximum lead diameter of 2.413 mm (0.095 in) and stackable on lead centers of 1.27 mm (0.050 in).

Contacting Tektronix

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Technical support	Email: techsupport@tektronix.com 1-800-833-9200, select option 3* 6:00 a.m. - 5:00 p.m. Pacific time

* **This phone number is toll free in North America. After office hours, please leave a voice mail message.**
Outside North America, contact a Tektronix sales office or distributor; see the Tektronix web site for a list of offices.

Operating Basics

This section provides a brief description of the Tektronix P6960 and P6980 Logic Analyzer Probes, information on attaching color-coded probe labels, and probe and adapter connection instructions from the logic analyzer to the target system.

Product Description

The P6960 and P6980 Logic Analyzer Probes connect TLA7Axx and TLA7NAx Series Logic Analyzer modules to a target system. The P6960 probe consists of 34 single-ended channels in one probe head, while the P6980 probe consists of 34 channels in two probe heads, with each head containing 17 differential channels.

Attaching Probe Labels

If you purchase probes for the logic analyzer module, you will need to apply the color-coded labels. You will find instructions on how to attach the labels to the probes on a color reference card that is included with the probes:

- *P6960 High Density Logic Analyzer Probe Labeling and Installation Instructions*
- *P6980 High Density Differential Logic Analyzer Probe Labeling and Installation Instructions*

The instructions are also included on the Documentation CD that ships with the probes.

P6960 High-Density Probe

The P6960 Probe is a 34-channel, high-density connectorless probe with D-Max probing technology (see Figure 1). The probe consists of one probe head that has 34 channels (32 data and 2 clock/qual).

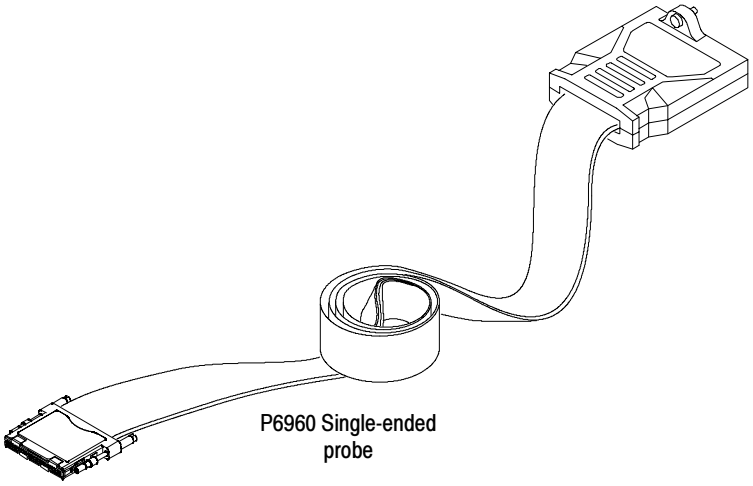

Figure 1: P6960 High-Density probe with D-Max probing technology

The following list details the capabilities and qualities of the P6960 Probe:

- Differential or single-ended clock and qualification inputs
- Single-ended data inputs
- cLGA contact eliminates need for built-in connector
- Footprint supports direct signal pass-through
- Supports PCB thickness of 1.27 mm to 6.35 mm (0.050 in to 0.250 in)
- Consists of one independent probe head of 34 channels (32 data and 2 clock/quals)
- Narrow 34-channel probe head makes for easier placement and layout
- 2X mode, (for example, 1:2 demultiplexing) uses one-half of the probe head
- 4X mode, (for example, 1:4 demultiplexing) uses one-quarter of the probe head
- Color-coded keyed attachment
- –2.5 V to +5 V input operating range
- –2.0 V to +4.5 V threshold range

- 300 mV minimum single-ended signal amplitude
- 150 mV amplitude each side minimum differential signal
- Minimal loading of 0.5 pF typical @ 20 kΩ to ground
- Operation in normal or inverted polarity is acceptable (clock only)
- Any common mode voltage is acceptable so long as the maximum positive voltage does not exceed +5 V and the maximum negative voltage does not exceed –2.5 V (clock only)

***NOTE**. Refer to Figure 15 on page 22 for P6960 probe routing and pin out information.*

P6980 High-Density Differential Probe

The P6980 Probe is a 34-channel, high-density connectorless differential probe with D-Max probing technology (see Figure 2). The probe consists of two independent probe heads of 17 channels each (16 data and 1 clock/qual).

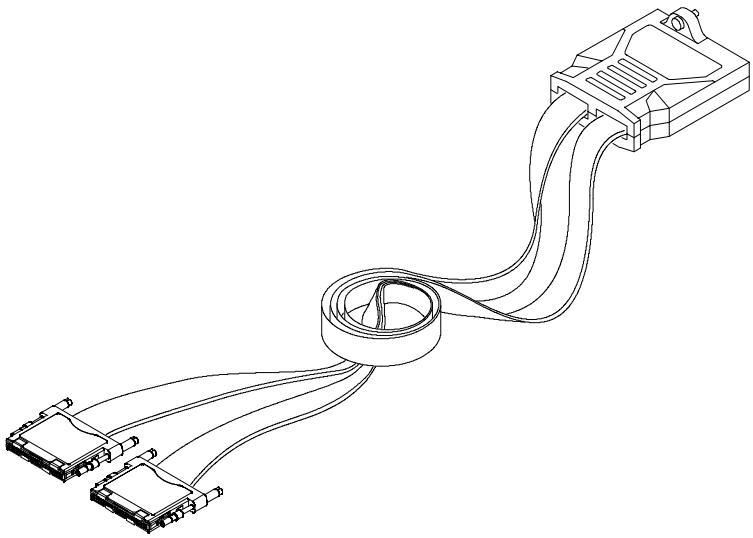

Figure 2: P6980 High-Density Differential probe with D-Max probing technology

The following list details the capabilities and qualities of the P6980 Probe:

- Differential data, clock and qualification inputs (single-ended signals may be probed if negative input is grounded)
- cLGA contact eliminates need for built-in connector
- Footprint supports direct signal pass-through
- Supports PCB thickness of 1.27 mm to 6.35 mm (0.050 in to 0.250 in)
- Consists of two probe heads supporting 17 channels each, for a total of 34 channels
- 2X mode (1:2 demultiplexing) and 4X mode (1:4 demultiplexing), use one probe head to minimize required board real estate
- Color-coded keyed attachment
- –2.5 V to +5 V input operating range
- –2.0 V to +4.5 V threshold range
- 300 mV minimum single-ended signal amplitude (5 V maximum)
- 150 mV each side minimum differential signal amplitude (2.5 V maximum)
- Minimal loading of 0.5 pF typical @ 20 kΩ to ground
- Operation in normal or inverted polarity is acceptable
- Any common mode voltage is acceptable so long as the maximum positive voltage does not exceed +5 V and the maximum negative voltage does not exceed –2.5 V

NOTE. *Refer to Figure 15 on page 22 for P6980 probe routing and pin out information.*

Connecting the Probes to the Logic Analyzer

Refer to Figure 3 and connect the probes to the logic analyzer according to the following steps.

1. Identify the beveled edges of the connector inside the module end of the probe.
2. Align the beveled edges of the connector to its mating connector on the logic analyzer module and press into place.
3. Use care to evenly tighten both screws on the module end of the probe until they are snug. First slightly tighten both screws, then snug each screw to 4 in-lbs (max).

***NOTE**. All P69xx series Logic Analyzer probes can be connected to the logic analyzer when it is powered on. In addition, all P69xx series Logic Analyzer probes connect to the logic analyzer in exactly the same manner.*

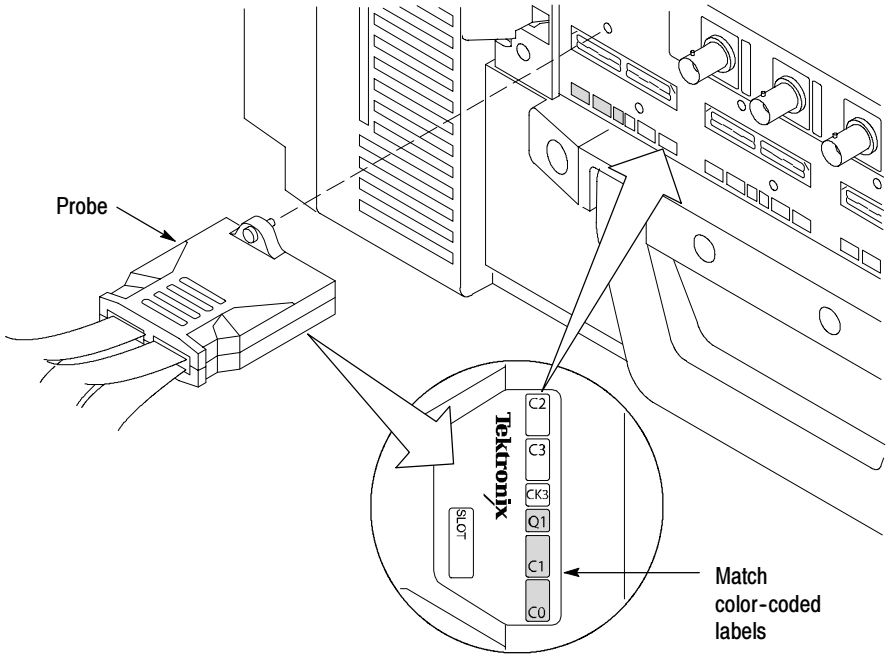

Figure 3: Connecting the probes to the logic analyzer

Connecting the Probes to the Target System

Connecting the P6960 High Density and P6980 Differential Probes

You can connect the P6960 High-Density and P6980 Differential Probes to the target system without turning off the power to the target system. The target system must have the probe retention posts installed; if your system does not have the posts, see the procedure below.

Using the Correct Retention Post Wires. If the PCB is ≤ .120 in thick, use the wire that comes preattached to the posts. If the PCB is > .120 in thick, use the longer wire that is included with the posts. To install the longer wires on the retention posts, refer to Figure 4 and do the following:

1. Remove the old wire by pulling the side of the wire over the retaining tab and lifting the wire away from the post.
2. Place the new wire in the slot side without the tab, and then wrap the wire over the tab side until it engages in the slot (you will feel or hear a slight click).

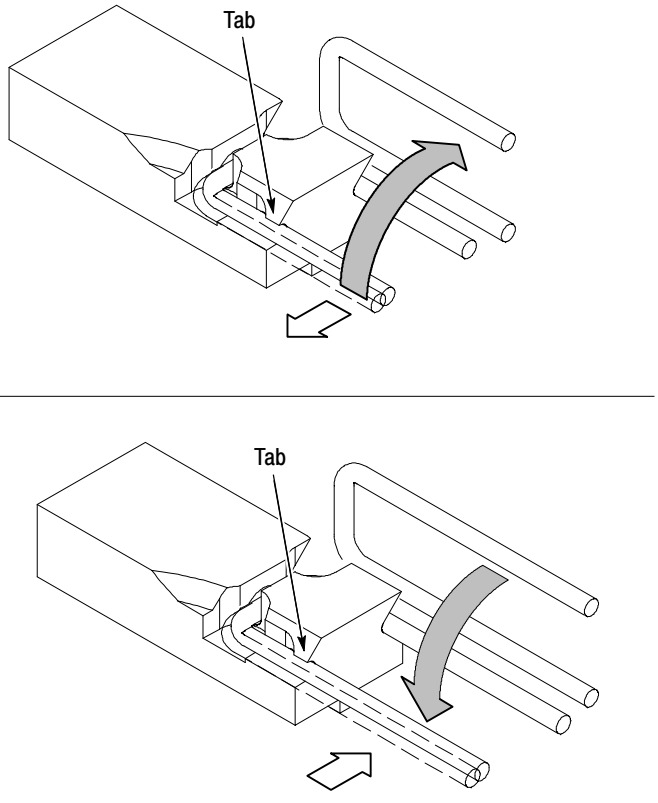

Figure 4: Replacing the wires on the retention posts

Installing the Retention Posts. To install the retention posts on the PCB, do the following:

1. On the retention post/carrier assembly, locate the black retention post (the post with the keying pin) and align it to the keying pin hole on the PCB. (See Figure 5.)

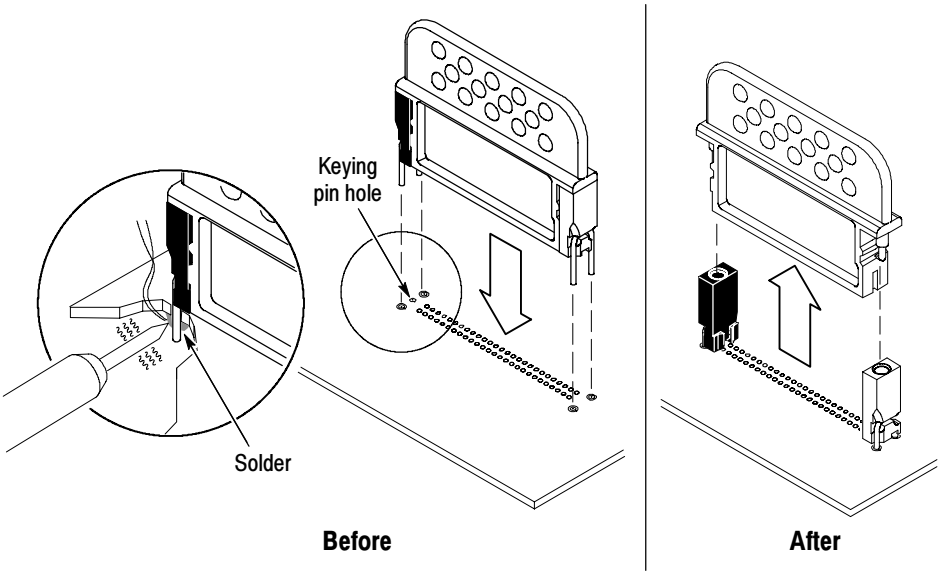

Figure 5: Aligning the retention posts to the PCB

2. Press the retention posts into the holes on the footprint on the PCB.
3. If your probing application will not be able to physically support (strain relieve) the probe cables, bend the post wires out to anchor the posts to the PCB. Ensure the assembly is perpendicular to the PCB when bending and soldering the post wires.
4. Solder the posts to the PCB. The posts can be soldered from the top or bottom of the circuit board.
5. Pull off the carrier from the posts.

Connect the Probe.

1. Align the black screw on the probe with the black post on the PCB. See Figure 6.

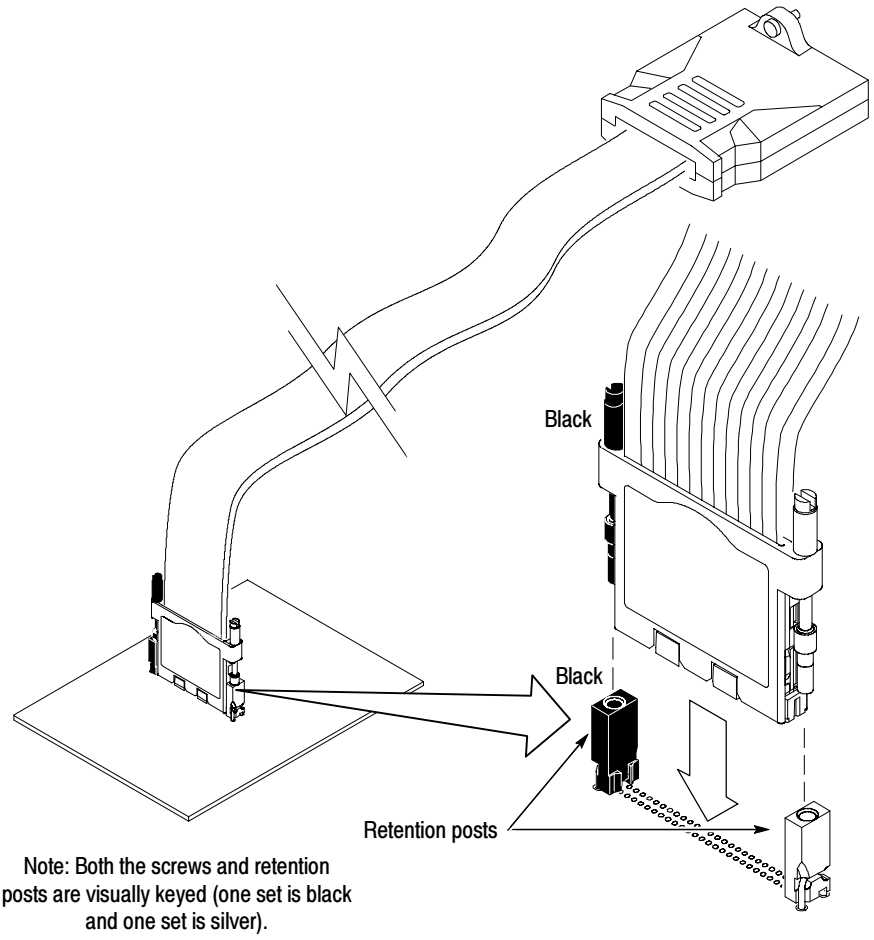

Figure 6: Connecting the probes to the target system

2. Secure the screws to the posts. If access is limited, use the adjustment tool that came with your probe. The probe is completely fastened to the PCB when the screws stop in the posts.

Connecting the Flying Leadset

The flying leadset, Tektronix part number 196-3494-XX, is an optional accessory for your probe. The flying leadset allows you to connect to individual test points on your PCB. However, for general-purpose probing, the P6810 probe is recommended for best performance.

Refer to Figure 7 and connect the probe to the target system by performing the steps that follow. You can connect the probe leads to the target system without turning off the power to the target system.

1. Connect the probe leads to the square pins on the PCB.
2. Connect the negative input to ground on the PCB.
3. Connect the leadset to the probe.

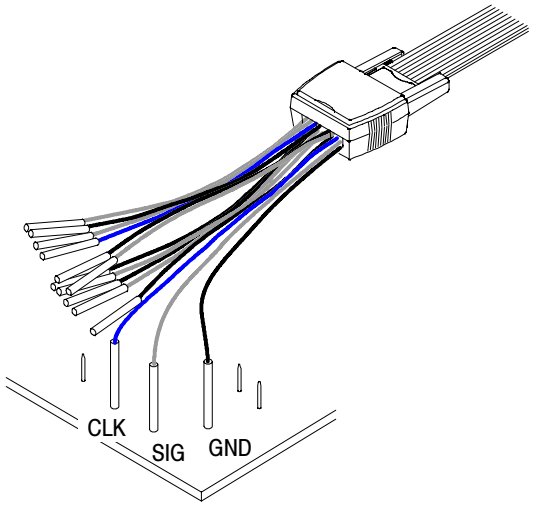

Figure 7: Using the flying leadset to connect to the target system

Dressing the Probe Cables

Use the Velcro cable managers to combine the cables together or to help relieve strain on the probe connections.

Hang the probe cables so that you relieve the tension on the probes at the retention posts. See Figure 8.

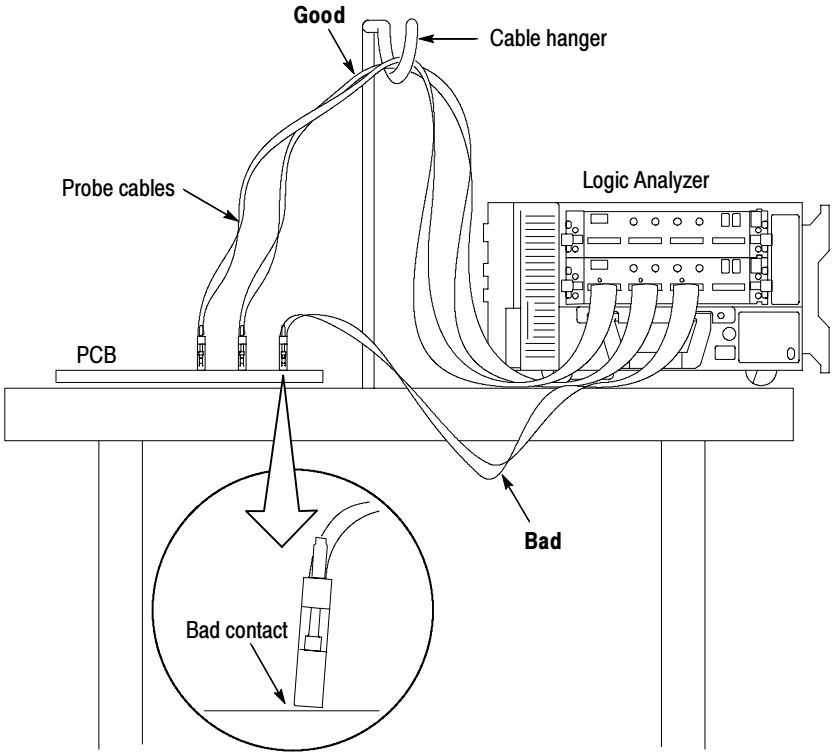

Figure 8: Proper dressing of the probe cables

Cleaning the Compression Footprints

The following procedure is optional, but recommended to obtain best performance.

CAUTION. *To avoid electrical damage, always turn off the power of your target system before cleaning the compression footprint.*

Prior to connecting the probe to the target system, the compression footprints on the board should be properly cleaned. Clean the compression footprints according to the following steps:

1. Use a lint-free cloth moistened with isopropyl alcohol and gently wipe the footprint surface.
2. Remove any remaining lint using a nitrogen air gun.

NOTE*. Use alcohol sparingly and be sure that you have removed any remaining lint or residue with the nitrogen air gun.*

Storing the Probe Heads

To protect the interface clip, it is important to properly store the probe heads when the probes are not in use. See Figure 9.

Gently slide the probe cover over the probe end and store the probe.

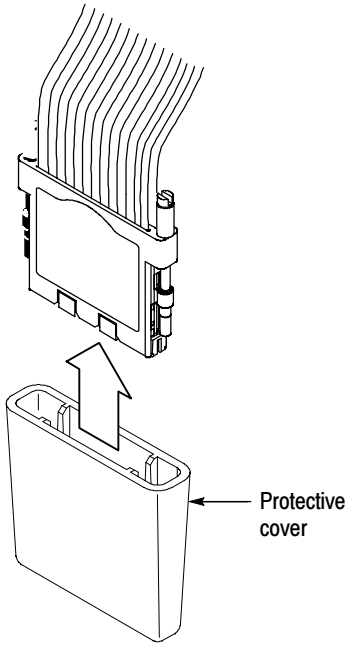

Figure 9: Protecting the probe heads

Reference

This section provides reference information for the P6960 High-Density and P6980 High-Density Differential Probes with D-Max probing technology. Topics include the following:

- Designing an interface between the probe and a target system
- Board design
- Probe footprint dimensions
- Probe pinout and channel assignment

Designing an Interface Between the Probes and a Target System

Once you have determined which probe is required, use the following information to design the appropriate connector into your target system board. The following topics are in this section:

- Signal fixturing considerations
- Signal connections (signal names and footprints)
- Mechanical considerations
- Electrical considerations

Signal Fixturing Considerations

This section contains the following information to consider for signal fixturing:

- Clocks and qualifiers
- Merged modules and source synchronous clocking
- Demultiplexing multiplexed buses
- 2X and 4X high resolution timing modes (Internal 2X and 4X)
- Probing analog signals
- Range recognition

Clocks and Qualifiers. Every logic analyzer has some special purpose input channels. Inputs designated as clocks can cause the analyzer to store data. Qualifier channels can be logically AND'ed and OR'ed with clocks to further define when the analyzer should latch data from the system under test. Routing the appropriate signals from your design to these inputs ensures that the logic analyzer can acquire data correctly. Unused clocks can be used as qualifier signals.

Depending on the channel width, each TLA7Axx and TLA7NAx Series logic analyzer module will have a different set of clock and qualifier channels. Table 1 shows the clock and qualifier channels available for each module.

Table 1: Logic analyzer clock and qualifier availability

TLA7Axx/ TLA7NAx Module	Clock Inputs				Qualifier Inputs			
	CLK:0	CLK:1	CLK:2	CLK:3	QUAL:0	QUAL:1	QUAL:2	QUAL:3
TLA7AA1	✓			✓				
TLA7AA2	✓	✓	✓	✓				
TLA7AA3	✓	✓	✓	✓	✓	✓		
TLA7AA4	✓	✓	✓	✓	✓	✓	✓	✓
TLA7AB2	✓	✓	✓	✓				
TLA7AB4	✓	✓	✓	✓	✓	✓	✓	✓
TLA7NA1	✓			✓				
TLA7NA2	✓	✓	✓	✓				
TLA7NA3	✓	✓	✓	✓	✓	✓		
TLA7NA4	✓	✓	✓	✓	✓	✓	✓	✓

All clock and qualifier channels are stored. The analyzer always stores the logic state of these channels every time it latches data.

Since clock and qualifier channels are stored in the analyzer memory there is no need to double probe these signals for timing analysis. When switching from state to timing analysis modes all of the clock and qualifier signals will be visible. This allows you to route signals not needed for clocking to the unused clock and qualifier channels.

It is a good practice to take advantage of the unused clock and qualifier channels to increase your options for when you will latch data. Routing several of your design's clocks and strobes to the analyzer clock inputs will provide you with a greater flexibility in the logic analyzer clocking setup menus.

As an example, look at a microprocessor with a master clock, data strobe, and an address strobe. Routing all three of these signals to analyzer clock inputs will enable you to latch data on the processor master clock, only when data is strobed, or only when address is strobed. Some forethought in signal routing can greatly expand the ways in which you can latch and analyze data.

A microprocessor also provides a good example of signals that can be useful as qualifiers. There are often signals that indicate data reads versus data writes (R/W), signals that show when alternate bus masters have control of the processor buses (DMA), and signals that show when various memory devices are being used (ChipSel). All of these signals are good candidates for assignment to qualifier channels.

By logically AND'ing the clock with one of these qualifiers you can program the analyzer to store only data reads or data writes. Using the DMA signal as a qualifier provides a means of filtering out alternate bus master cycles. Chip selects can limit data latching to specific memory banks, I/O ports, or peripheral devices.

Merged Module Sets and Source Synchronous Clocking. TLA7Axx and TLA7NAx analyzer modules that are 102 channels or 136 channels wide can be merged together to act as a single logic analyzer with a larger channel count. Up to five modules can be merged to provide up to a 680 channel analyzer. A unique feature of the TLA7Axx module is that it supports source synchronous clocking. Combining these two capabilities provide some additional considerations for signal routing.

Source synchronous clocking is a method that manages the skew between the system clock and the data bus by requiring the sending device to drive an actual clock or strobe signal along with the data that is very tightly coupled with it in terms of skew. The receiving device then uses this strobe to capture the data.

A variant of this scheme is being applied to large microprocessor buses, where the bus is split into smaller, more easily managed groups that each have their own dedicated strobe. Although the timing relationship between a particular clock and its associated data group is very tight, the timing between the different groups can vary greatly and changes depending on which device has control of the bus.

Many source synchronous designs use wide buses. It is not uncommon to require a set of merged logic analyzer modules to provide the channel count needed in probing larger source synchronous systems. While all of the modules in a merged set can use their clock inputs independently if needed, it must be remembered that there are a maximum of four clock inputs on a 136 channel wide module.

To see the importance of this reminder we will once again use a microprocessor system as an example. Tektronix logic analyzer processor has a 32 bit address bus and a 64 bit data bus. The data bus is split into four 16 bit subgroups that have independent source synchronous clocks. For the logic analyzer to correctly acquire data from this system it will need five clock inputs, one for the address bus and one each for the four 16 bit data bus subgroups.

To acquire both buses the analyzer would need at least 96 channels (32 address and 64 data). However, a single 102 channel card doesn't have the required five clock inputs. By merging two 102 channel modules into a set you can obtain the needed number of clock inputs. Route the address bus to one module in the set and route the data bus, along with its four source synchronous clocks, to the second module in the set.

Demultiplexing Multiplexed Buses. TLA7Axx modules support both 2X and 4X demultiplexing. TLA7NAx modules support 2X demultiplexing. Each signal on a dual or quad multiplexed bus can be demultiplexed into its own logic analyzer channel. See Tables 2 and 3 to determine the correct channel groups to use.

Table 2: 2X Demultiplexing source-to-destination channel assignments

Source connecting channel groups	Destination channels receiving target system test data					
	TLA7AA4/ TLA7NA4	TLA7AA3/ TLA7NA3	TLA7AA2/ TLA7NA2	TLA7AA1/ TLA7NA1	TLA7AB4	TLA7AB2
A3:7-0	D3:7-0	D3:7-0	C3:7-0	C3:7-0	D3:7-0	C3:7-0
A2:7-0	D2:7-0	D2:7-0	C2:7-0	C2:7-0	D2:7-0	C2:7-0
A1:7-0	D1:7-0	D1:7-0	D1:7-0		D1:7-0	D1:7-0
A0:7-0	D0:7-0	D0:7-0	D0:7-0		D0:7-0	D0:7-0
C3:7-0	C1:7-0	C1:7-0			C1:7-0	
C2:7-0	C0:7-0	C0:7-0			C0:7-0	
E3:7-0	E1:7-0				E1:7-0	
E2:7-0	E0:7-0				E0:7-0	
CLK:0	QUAL:1	QUAL:1			QUAL:1	
CLK:1	QUAL:0	QUAL:0			QUAL:0	
CLK:2	QUAL:3				QUAL:3	
CLK:3	QUAL:2				QUAL:2	

Table 3: 4X Demultiplexing source-to-destination channel assignments

Source connecting channel groups	Destination channels receiving target system test data					
	TLA7AA4	TLA7AA3	TLA7AA2	TLA7AA1	TLA7AB4	TLA7AB2
C3:7-0	C2:7-0 C1:7-0 C0:7-0	C2:7-0 C1:7-0 C0:7-0	A3:7-0 A2:7-0 C2:7-0	A3:7-0 A2:7-0 C2:7-0	C2:7-0 C1:7-0 C0:7-0	A3:7-0 A2:7-0 C2:7-0
A1:7-0	A0:7-0 D1:7-0 D0:7-0	A0:7-0 D1:7-0 D0:7-0	A0:7-0 D1:7-0 D0:7-0		A0:7-0 D1:7-0 D0:7-0	A0:7-0 D1:7-0 D0:7-0
A3:7-0	A2:7-0 D3:7-0 D2:7-0	A2:7-0 D3:7-0 D2:7-0			A2:7-0 D3:7-0 D2:7-0	
E3:7-0	E2:7-0 E1:7-0 E0:7-0				E2:7-0 E1:7-0 E0:7-0	
CLK:3	CLK:2 QUAL:3 QUAL:2				CLK:2 QUAL:3 QUAL:2	
CLK:1	CLK:0 QUAL:1 QUAL:0	CLK:0 QUAL:1 QUAL:0			CLK:0 QUAL:1 QUAL:0	

When demultiplexing data there is no need to connect the destination channels to the multiplexed bus. Data from the source channels are routed to the destination channels internal to the logic analyzer. Tables 2 and 3 show the mapping of source channels to destination channels.

Demultiplexing affects only the main memory for the destination channels. This means that the MagniVu memory is filled with data from whatever is connected to the demultiplexing destination channel probe inputs. This provides an opportunity to acquire high resolution MagniVu data on a few extra channels. Connecting the demultiplexing destination channels to other signals will allow viewing of their activity in the MagniVu memory but not the main memory.

2X and 4X High Resolution Timing Modes. 2X high resolution timing mode provides double the normal 500 MHz sample rate on one-half of the channels. By trading half of the analyzer's channels, the remaining channels can be sampled at a 1 GHz rate with double the memory depth. Likewise, 4X high resolution timing mode provides quadruple the normal 500 MHz sample rate on one-fourth of the channels. By trading three-fourths of the analyzer's channels, the remaining channels can be sampled at a 2 GHz rate with quadruple the memory depth.

Both of the high resolution timing modes use the same demultiplexing channel routing as shown in Tables 2 and 3. By taking care to assign critical signals to the demultiplexing source channels, you can obtain extra timing resolution where it is most needed. Since demultiplexing affects only the main memory you will still have the MagniVu data available for all of the signals that are disconnected from the main memory when you switch to the high resolution timing modes.

Probing Analog Signals. The TLA7Axx module provides visibility of analog signals with Analog mux. Analog mux routes the actual signal seen by each channel's probe through a high bandwidth path to an analog multiplexer inside of the logic analyzer module. From the logic analyzer interface you can route any input channel to one of four output connectors on the module. By connecting the analyzer analog outputs to your oscilloscope you can see the analog characteristics of any signal probed by the logic analyzer.

Sometimes it is convenient to have analog signals accessible for easier probing. Signals such as A/D Converter inputs, D/A Converter outputs, low voltage power supplies, termination voltages, and oscillator outputs are just a few examples. Routing these signals to unused logic analyzer inputs provides a quick method of viewing their activity without ever picking up an oscilloscope probe.

Care must be taken to ensure that such signals are voltage limited and will not exceed the maximum nondestructive input voltage for the logic analyzer probes of ±15 Vpeak.

Range Recognition. When using range recognizers, the probe groups and probe channels must be in hardware order. Probe groups must be used from the most-significant probe group to the least-significant probe group based on the following order:

C3 C2 C1 C0 E3 E2 E1 E0 A3 A2 D3 D2 A1 A0 D1 D0 Q3 Q2 Q1 Q0 CK3 CK2 CK1 CK0

Probe channels must be from the most-significant channel to the least-significant channel based on the following order:

7 6 5 4 3 2 1 0

The above examples assumes a 136-channel LA module. The missing channels in LA modules with fewer than 136 channels are ignored. With merged modules, range recognition extends across the first three modules: the master module contains the most-significant channels.

Board Design

This section provides information that helps you design your PCB mechanically and electrically for use with the P69XX logic analyzer probes.

Probe Dimensions

Figure 10 shows the probe dimensions for the P6960 and P6980 probes.

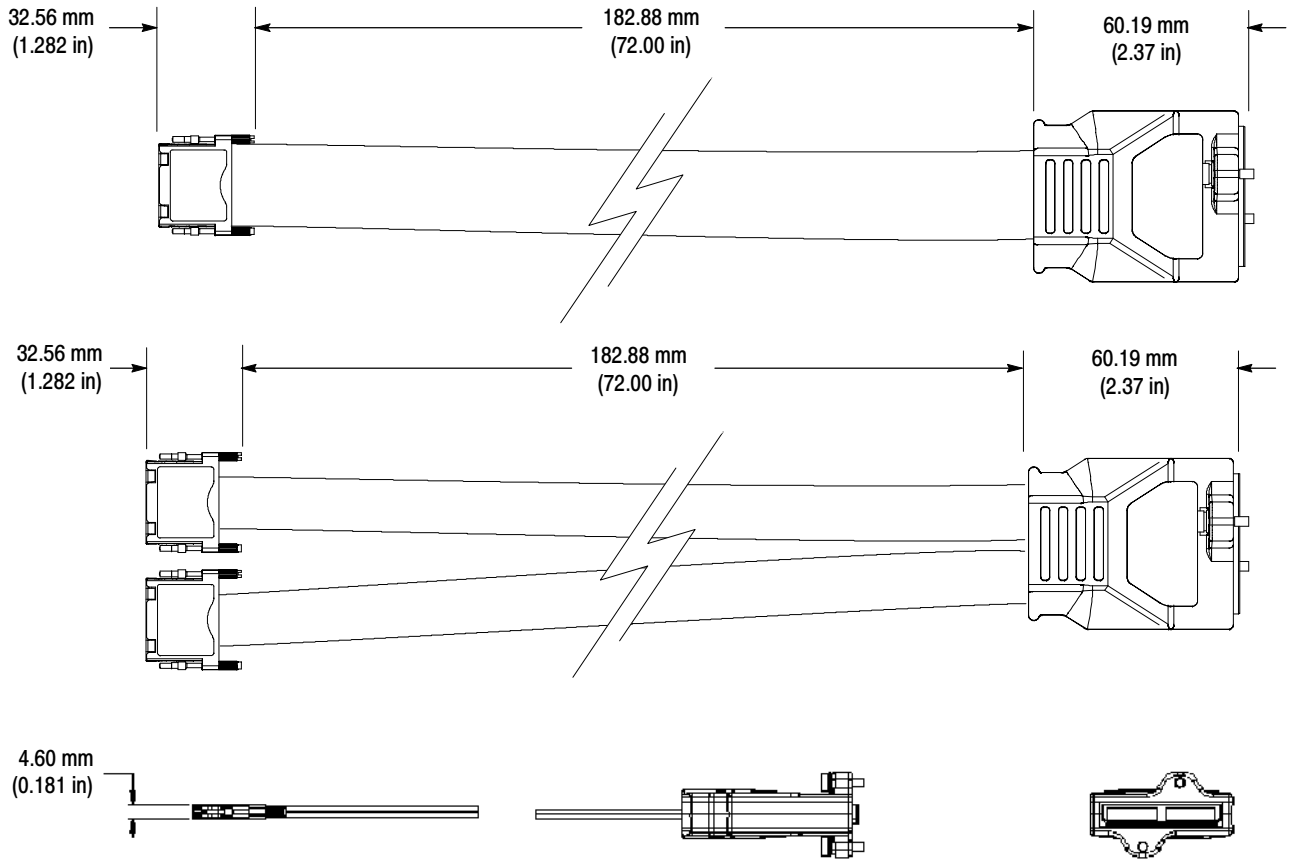

Figure 10: P6960 and P6980 probe dimensions

Retention Post Dimensions and Keep out

The probes are attached to the PC board using two retention posts which ensures a reliable electrical and mechanical connection to your design, pin-to-pad alignment, and holds the probe securely to the board. Board thicknesses that are supported include 1.27 mm (0.050 in) to 6.35 mm (0.250 in). Figure 11 shows the dimensions of the retention posts.

CAUTION. *To avoid solder creep, bend the post wires out after you insert the posts in the board, and then solder the post wires. You can solder the retention wires from the top or bottom of the circuit board.*

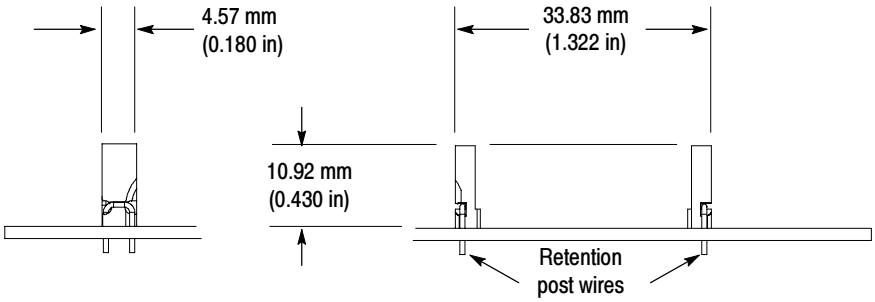

Figure 11: Retention post dimensions

Figure 12 shows the keep out area required for the retention posts. Vias must be placed outside of the keep out area. Any traces routed on the top layer of the board must stay outside of the keepout area. Traces may be routed on inner layers of the board through the keepout area.

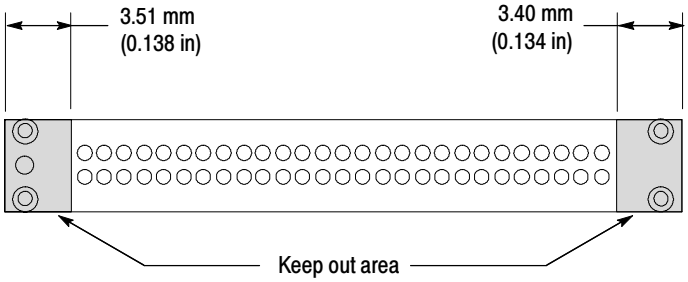

Figure 12: Keep out area

Side-by-side and End-to-end Layout Dimensions

Figure 13 shows the dimensions for side-by-side footprint layout.

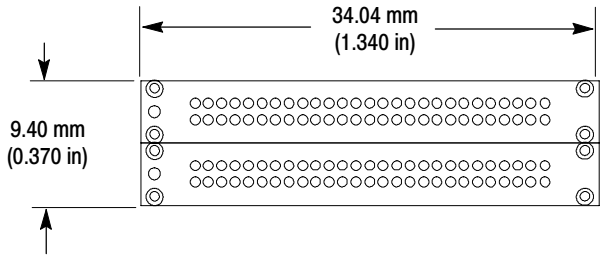

Figure 13: Side-by-side layout

Figure 14 shows the dimensions for an end-to-end footprint layout.

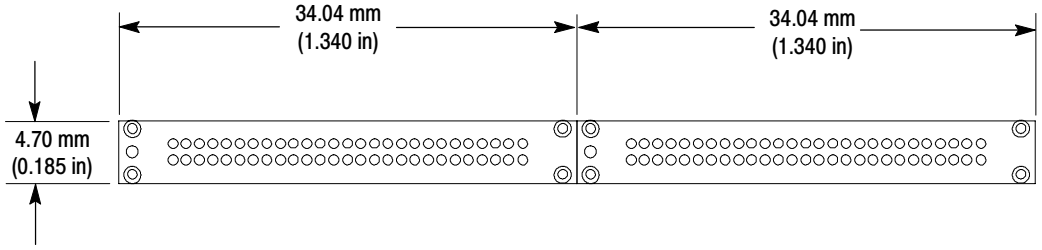

Figure 14: End-to-end layout

Signal Routing

Figure 15 shows examples of pass through signal routing for a single-ended data configuration and a differential data configuration.

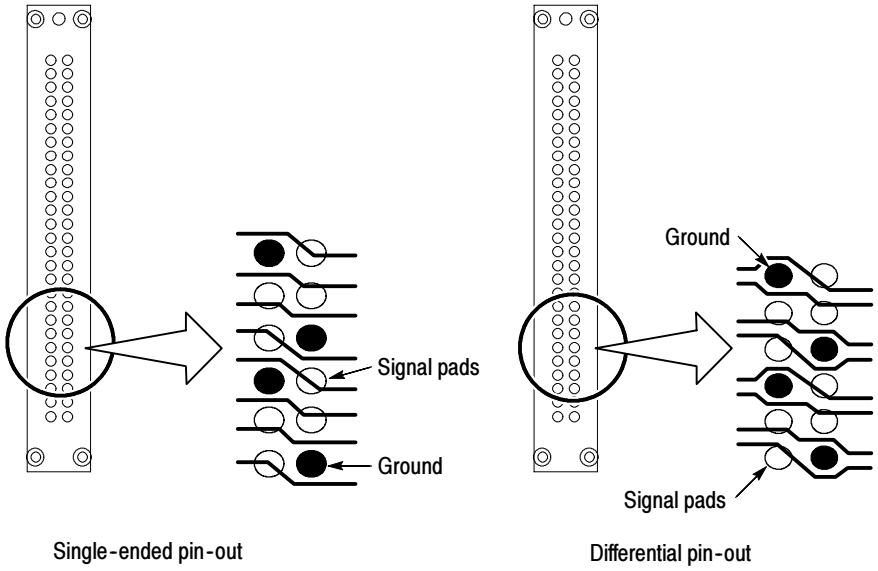

Figure 15: Signal routing on the target system

Mechanical Considerations

This section provides information on compression footprint requirements and physical attachment requirements.

The PCB holes, in general, do not have an impact upon the integrity of your signals when the signals routed around the holes have the corresponding return current plane immediately below the signal trace for the entire signal path from driver to receiver.

***NOTE**. For optimum signal integrity, there should be a continuous, uninterrupted ground return plane along the entire signal path.*

Physical Attachment Requirements for the P6960 and P6980 Probes. The P6960 High-Density Probe and P6980 High-Density Differential Probe interconnects are designed to accommodate PCB thickness ranging from 1.27 mm to 6.35 mm (0.050 in to 0.250 in). To accommodate this range, there are two wire lengths in the design:

- For board thicknesses of 0.050 in to 0.120 in, use the standard wire that is mounted to the post
- For board thicknesses of 0.120 in to 0.250 in, use the long wire supplied with the probe

For more information, see *Using the Correct Retention Post Wires* on page 6.

Electrical Considerations

This section provides information on transmission lines and load models for the P6960 High-Density, and P6980 High-Density Differential Probes.

The low frequency model is typically adequate for rise and fall times of 1 ns or slower in a typical 25 Ω source impedance environment (50 Ω runs with a pass-through connection). For source impedance outside this range, and/or rise and fall times faster than 1 ns, use the high frequency model to determine if a significant difference is obtained in the modeling result.

The compression land pattern pad is not part of the load model. Make sure that you include the compression land pad in the modeling.

Transmission Lines. Due to the high performance nature of the interconnect, ensure that stubs, which are greater than 1/4 length of the signal rise time, are modeled as transmission lines.

P6960 High-Density and P6980 High-Density Differential Probes Load Model. The following electrical model (see Figure 16) includes a low-frequency and high-frequency model of the High-Density and High-Density Differential Probes. For the Differential Probe, the load model is applied to both the + side and the – side of the signal.

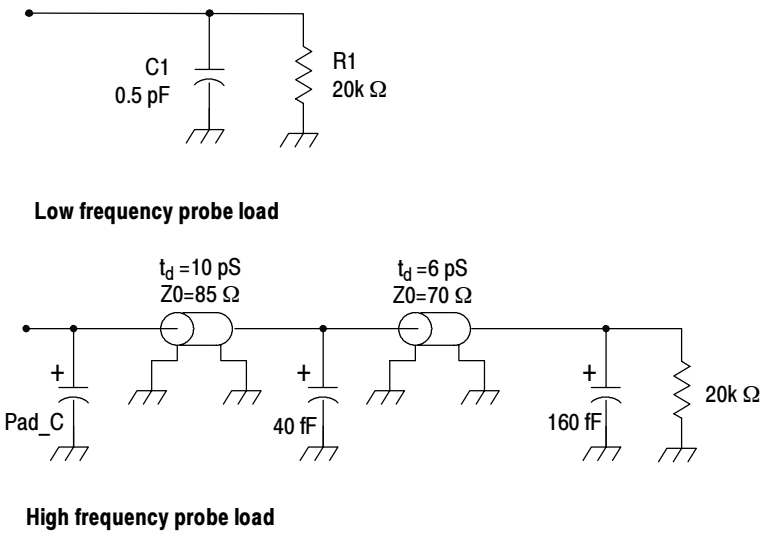

Figure 16: High-Density and High-Density Differential probe load model

The differential load for the P6960 clock input and the P6980 probe can be modeled by attaching the single line model to each side (+ and –) of the differential signal. The + and – sides of the differential signal are well insulated in the probe head up to and including the differential input stage.

Probe Footprint Dimensions

Use the probe footprint dimensions in Figure 17 to lay out your circuit board pads and holes for attaching the retention posts. Pad finishes that are supported include immersion gold, immersion silver, and hot air solder level.

***NOTE**. Tektronix recommends using immersion gold surface finish for best performance.*

Tektronix also recommends that the probe attachment holes float or remain unconnected to a ground plane. This prevents overheating the ground plane and promotes quicker soldering of the retention posts to your PCB. The probe retention posts are designed to allow you to solder the retention posts from either side of your PCB.

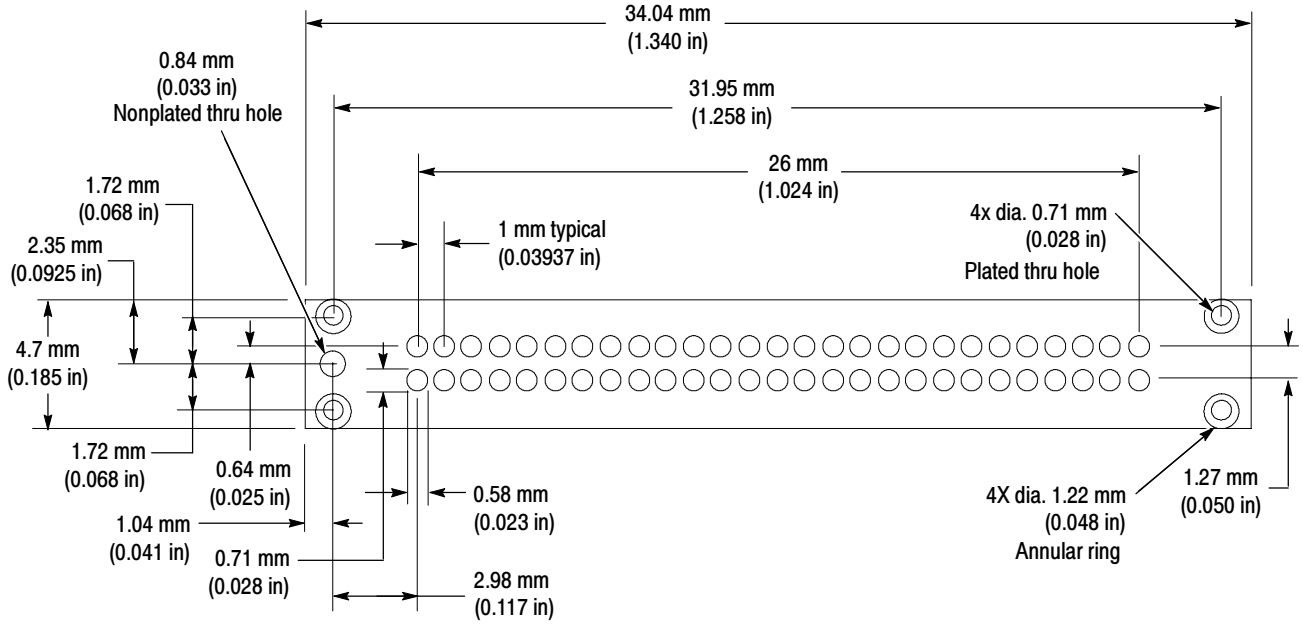

Figure 17: Probe footprint dimensions on the PCB

***NOTE**. You must maintain a solder mask web between the pads when traces are routed between pads on the same layer. The solder mask must not encroach onto the pads within the pad dimensions shown in Figure 12 on page 20.*

Other Design Considerations

Via-in-pad

Traditional layout techniques require vias to be located next to a pad and a signal routed to the pad, causing a stub and more PCB board area to be used for the connection. Many of today's new digital designs require you to minimize the electrical effects of the logic analyzer probing that you design into the circuit board. Using via-in-pad to route signals to the pads on the circuit board allows you to minimize the stub length of the signals on your board, thus providing the smallest intrusion to your signals. It also enables you to minimize the board area that is used for the probe footprint and maintain the best electrical performance of your design.

Figure 18 shows a footprint example where two pads use vias. Detail A describes the recommended position of the via with respect to the pad.

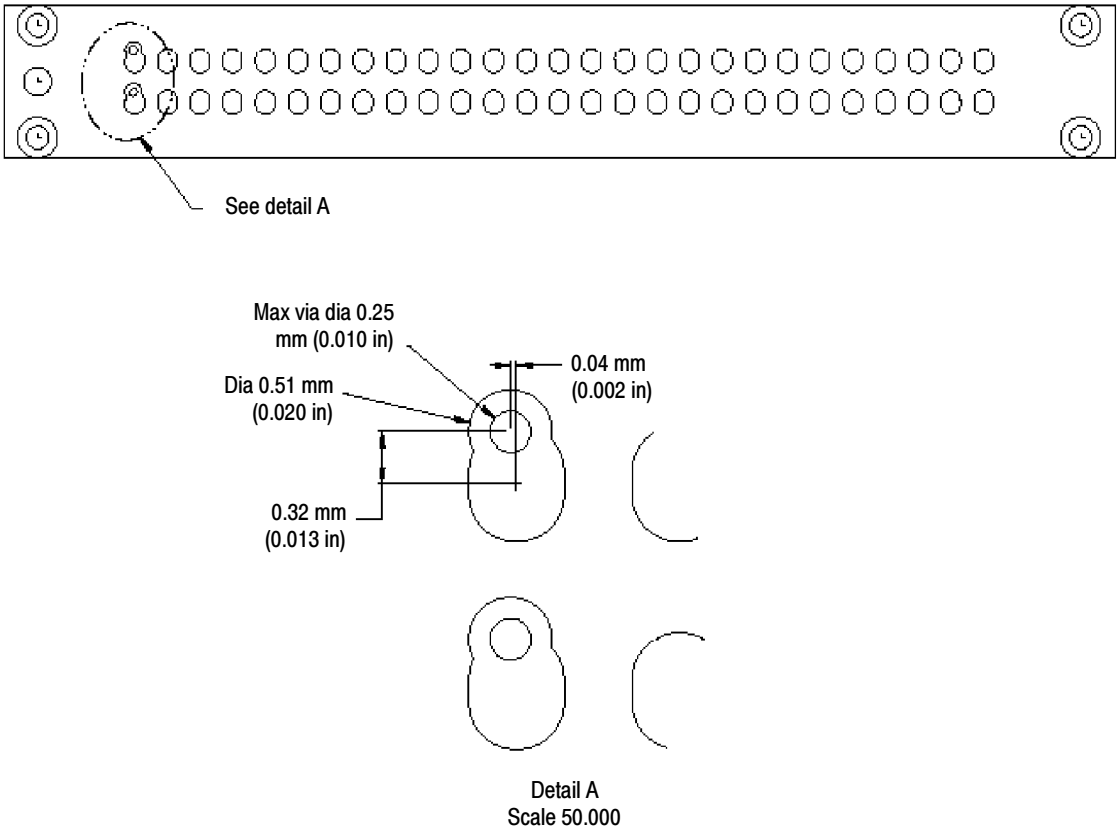

Figure 18: Optional Via-in-Pad placement recommendation

Probe Pinout Definition and Channel Assignment

This section contains probe pinout definitions and channel assignment tables for P6960 and P6980 probes.

P6960 Single-ended Probe with D-Max probing technology

Figure 19 shows the pad assignments, pad numbers, and signal names for the P6960 single-ended data, differential clock logic analyzer probe. The P6960 probe has 32 data channels, one clock, and one qualifier for each footprint.

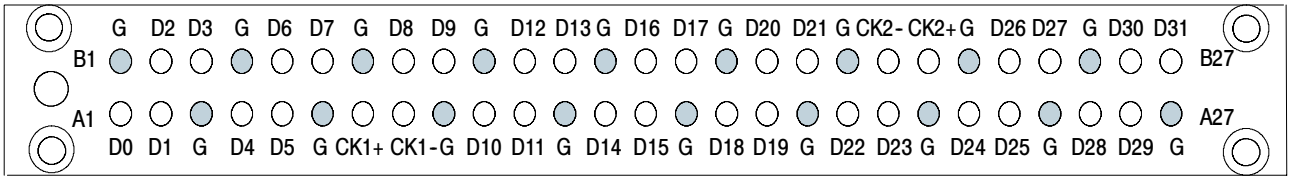

Figure 19: P6960 single-ended pinout detail

Table 4 on page 28 lists the channel mapping to a logic analyzer module for a P6960 single-ended data, differential clock logic analyzer probe.

Table 4: Channel assignment for a P6960 single-ended data, differential clock logic analyzer probe

		136 Channel				68 Channel	
			102 Channel				34 Channel
Pin Number	Signal name	Probe4	Probe 3	Probe 2	Probe 1	Probe 2	Probe 1
A1	D0	E2:0	A2:0	A0:0	C2:0	A0:0	C2:0
A2	D1	E2:1	A2:1	A0:1	C2:1	A0:1	C2:1
A3	GND	GND	GND	GND	GND	GND	GND
A4	D4	E2:4	A2:4	A0:4	C2:4	A0:4	C2:4
A5	D5	E2:5	A2:5	A0:5	C2:5	A0:5	C2:5
A6	GND	GND	GND	GND	GND	GND	GND
A7	CK1+	Q3+	CK0+	CK1+	CK3+	CK1+	CK3+
A8	CK1-	Q3-	CK0-	CK1-	CK3-	CK1-	CK3-
A9	GND	GND	GND	GND	GND	GND	GND
A10	D10	E3:2	A3:2	A1:2	C3:2	A1:2	C3:2
A11	D11	E3:3	A3:3	A1:3	C3:3	A1:3	C3:3
A12	GND	GND	GND	GND	GND	GND	GND
A13	D14	E3:6	A3:6	A1:6	C3:6	A1:6	C3:6
A14	D15	E3:7	A3:7	A1:7	C3:7	A1:7	C3:7
A15	GND	GND	GND	GND	GND	GND	GND
A16	D18	E1:5	D3:5	D1:5	C1:5	D1:5	A3:5
A17	D19	E1:4	D3:4	D1:4	C1:4	D1:4	A3:4
A18	GND	GND	GND	GND	GND	GND	GND
A19	D22	E1:1	D3:1	D1:1	C1:1	D1:1	A3:1
A20	D23	E1:0	D3:0	D1:0	C1:0	D1:0	A3:0
A21	GND	GND	GND	GND	GND	GND	GND
A22	D24	E0:7	D2:7	D0:7	C0:7	D0:7	A2:7
A23	D25	E0:6	D2:6	D0:6	C0:6	D0:6	A2:6
A24	GND	GND	GND	GND	GND	GND	GND
A25	D28	E0:3	D2:3	D0:3	C0:3	D0:3	A2:3
A26	D29	E0:2	D2:2	D0:2	C0:2	D0:2	A2:2
A27	GND	GND	GND	GND	GND	GND	GND

Table 4: Channel assignment for a P6960 single-ended data, differential clock logic analyzer probe (Cont.)

		136 Channel				68 Channel	
			102 Channel				34 Channel
Pin Number	Signal name	Probe4	Probe 3	Probe 2	Probe 1	Probe 2	Probe 1
B1	GND	GND	GND	GND	GND	GND	GND
B2	D2	E2:2	A2:2	A0:2	C2:2	A0:2	C2:2
B3	D3	E2:3	A2:3	A0:3	C2:3	A0:3	C2:3
B4	GND	GND	GND	GND	GND	GND	GND
B5	D6	E2:6	A2:6	A0:6	C2:6	A0:6	C2:6
B6	D7	E2:7	A2:7	A0:7	C2:7	A0:7	C2:7
B7	GND	GND	GND	GND	GND	GND	GND
B8	D8	E3:0	A3:0	A1:0	C3:0	A1:0	C3:0
B9	D9	E3:1	A3:1	A1:1	C3:1	A1:1	C3:1
B10	GND	GND	GND	GND	GND	GND	GND
B11	D12	E3:4	A3:4	A1:4	C3:4	A1:4	C3:4
B12	D13	E3:5	A3:5	A1:5	C3:5	A1:5	C3:5
B13	GND	GND	GND	GND	GND	GND	GND
B14	D16	E1:7	D3:7	D1:7	C1:7	D1:7	A3:7
B15	D17	E1:6	D3:6	D1:6	C1:6	D1:6	A3:6
B16	GND	GND	GND	GND	GND	GND	GND
B17	D20	E1:3	D3:3	D1:3	C1:3	D1:3	A3:3
B18	D21	E1:2	D3:2	D1:2	C1:2	D1:2	A3:2
B19	GND	GND	GND	GND	GND	GND	GND
B20	CK2-	Q2-	Q0-	CK2-	Q1-	CK2-	CK0-
B21	CK2+	Q2+	Q0+	CK2+	Q1+	CK2+	CK0+
B22	GND	GND	GND	GND	GND	GND	GND
B23	D26	E0:5	D2:5	D0:5	C0:5	D0:5	A2:5
B24	D27	E0:4	D2:4	D0:4	C0:4	D0:4	A2:4
B25	GND	GND	GND	GND	GND	GND	GND
B26	D30	E0:1	D2:1	D0:1	C0:1	D0:1	A2:1
B27	D31	E0:0	D2:0	D0:0	C0:0	D0:0	A2:0

P6980 Differential Probe with D-Max probing technology

Figure 20 shows the pad assignments, pad numbers, and signal names for the P6980 differential data and clock logic analyzer probe. The P6980 probe has 16 data channels, and one clock or qualifier for each footprint. There are two footprints associated with one P6980 probe.

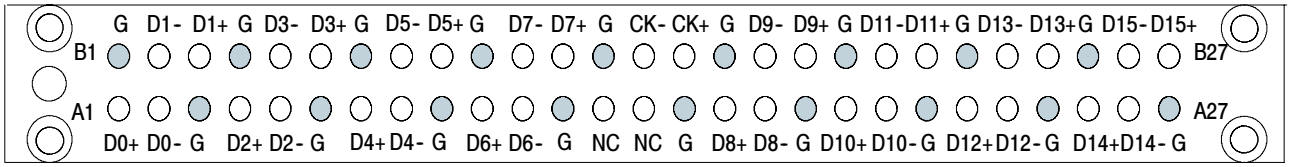

Figure 20: P6980 differential pinout detail

Table 5 on page 31 lists the channel mapping to a 136 channel or 102 channel logic analyzer module for the P6980 differential data and clock logic analyzer probe.

Table 5: Channel assignment for a P6980 differential clock and data logic analyzer probe to a 136 or 102 channel logic analyzer module

		136 Channel							
				102 Channel					
		Probe 4		Probe 3		Probe 2		Probe 1	
Pin number	Signal name	Head1	Head2	Head1	Head2	Head1	Head2	Head1	Head2
A1	D0+	E2:0+	E0:0+	A2:0+	D2:0+	A0:0+	D0:0+	C2:0+	C0:0+
A2	D0-	E2:0-	E0:0-	A2:0-	D2:0-	A0:0-	D0:0-	C2:0-	C0:0-
A3	GND	GND	GND	GND	GND	GND	GND	GND	GND
A4	D2+	E2:2+	E0:2+	A2:2+	D2:2+	A0:2+	D0:2+	C2:2+	C0:2+
A5	D2-	E2:2-	E0:2-	A2:2-	D2:2-	A0:2-	D0:2-	C2:2-	C0:2-
A6	GND	GND	GND	GND	GND	GND	GND	GND	GND
A7	D4+	E2:4+	E0:4+	A2:4+	D2:4+	A0:4+	D0:4+	C2:4+	C0:4+
A8	D4-	E2:4-	E0:4-	A2:4-	D2:4-	A0:4-	D0:4-	C2:4-	C0:4-
A9	GND	GND	GND	GND	GND	GND	GND	GND	GND
A10	D6+	E2:6+	E0:6+	A2:6+	D2:6+	A0:6+	D0:6+	C2:6+	C0:6+
A11	D6-	E2:6-	E0:6-	A2:6-	D2:6-	A0:6-	D0:6-	C2:6-	C0:6-
A12	GND	GND	GND	GND	GND	GND	GND	GND	GND
A13	NC	NC	NC	NC	NC	NC	ND	NC	NC
A14	NC	NC	NC	NC	NC	NC	ND	NC	NC
A15	GND	GND	GND	GND	GND	GND	GND	GND	GND
A16	D8+	E3:0+	E1:0+	A3:0+	D3:0+	A1:0+	D1:0+	C3:0+	C1:0+
A17	D8-	E3:0-	E1:0-	A3:0-	D3:0-	A1:0-	D1:0-	C3:0-	C1:0-
A18	GND	GND	GND	GND	GND	GND	GND	GND	GND
A19	D10+	E3:2+	E1:2+	A3:2+	D3:2+	A1:2+	D1:2+	C3:2+	C1:2+
A20	D10-	E3:2-	E1:2-	A3:2-	D3:2-	A1:2-	D1:2-	C3:2-	C1:2-
A21	GND	GND	GND	GND	GND	GND	GND	GND	GND
A22	D12+	E3:4+	E1:4+	A3:4+	D3:4+	A1:4+	D1:4+	C3:4+	C1:4+
A23	D12-	E3:4-	E1:4-	A3:4-	D3:4-	A1:4-	D1:4-	C3:4-	C1:4-
A24	GND	GND	GND	GND	GND	GND	GND	GND	GND
A25	D14+	E3:6+	E1:6+	A3:6+	D3:6+	A1:6+	D1:6+	C3:6+	C1:6+
A26	D14-	E3:6-	E1:6-	A3:6-	D3:6-	A1:6-	D1:6-	C3:6-	C1:6-
A27	GND	GND	GND	GND	GND	GND	GND	GND	GND

Table 5: Channel assignment for a P6980 differential clock and data logic analyzer probe to a 136 or 102 channel logic analyzer module (Cont.)

		136 Channel							
				102 Channel					
		Probe 4		Probe 3		Probe 2		Probe 1	
Pin number	Signal name	Head1	Head2	Head1	Head2	Head1	Head2	Head1	Head2
B1	GND	GND	GND	GND	GND	GND	GND	GND	GND
B2	D1-	E2:1-	E0:1-	A2:1-	D2:1-	A0:1-	D0:1-	C2:1-	C0:1-
B3	D1+	E2:1+	E0:1+	A2:1+	D2:1+	A0:1+	D0:1+	C2:1+	C0:1+
B4	GND	GND	GND	GND	GND	GND	GND	GND	GND
B5	D3-	E2:3-	E0:3-	A2:3-	D2:3-	A0:3-	D0:3-	C2:3-	C0:3-
B6	D3+	E2:3+	E0:3+	A2:3+	D2:3+	A0:3+	D0:3+	C2:3+	C0:3+
B7	GND	GND	GND	GND	GND	GND	GND	GND	GND
B8	D5-	E2:5-	E0:5-	A2:5-	D2:5-	A0:5-	D0:5-	C2:5-	C0:5-
B9	D5+	E2:5+	E0:5+	A2:5+	D2:5+	A0:5+	D0:5+	C2:5+	C0:5+
B10	GND	GND	GND	GND	GND	GND	GND	GND	GND
B11	D7-	E2:7-	E0:7-	A2:7-	D2:7-	A0:7-	D0:7-	C2:7-	C0:7-
B12	D7+	E2:7+	E0:7+	A2:7+	D2:7+	A0:7+	D0:7+	C2:7+	C0:7+
B13	GND	GND	GND	GND	GND	GND	GND	GND	GND
B14	CK-	Q3-	Q2-	CK0-	Q0-	CK1-	CK2-	CK3-	Q1-
B15	CK+	Q3+	Q2+	CK0+	Q0+	CK1+	CK2+	CK3+	Q1+
B16	GND	GND	GND	GND	GND	GND	GND	GND	GND
B17	D9-	E3:1-	E1:1-	A3:1-	D3:1-	A1:1-	D1:1-	C3:1-	C1:1-
B18	D9+	E3:1+	E1:1+	A3:1+	D3:1+	A1:1+	D1:1+	C3:1+	C1:1+
B19	GND	GND	GND	GND	GND	GND	GND	GND	GND
B20	D11-	E3:3-	E1:3-	A3:3-	D3:3-	A1:3-	D1:3-	C3:3-	C1:3-
B21	D11+	E3:3+	E1:3+	A3:3+	D3:3+	A1:3+	D1:3+	C3:3+	C1:3+
B22	GND	GND	GND	GND	GND	GND	GND	GND	GND
B23	D13-	E3:5-	E1:5-	A3:5-	D3:5-	A1:5-	D1:5-	C3:5-	C1:5-
B24	D13+	E3:5+	E1:5+	A3:5+	D3:5+	A1:5+	D1:5+	C3:5+	C1:5+
B25	GND	GND	GND	GND	GND	GND	GND	GND	GND
B26	D15-	E3:7-	E1:7-	A3:7-	D3:7-	A1:7-	D1:7-	C3:7-	C1:7-
B27	D15+	E3:7+	E1:7+	A3:7+	D3:7+	A1:7+	D1:7+	C3:7+	C1:7+

Table 6 lists the channel mapping to a 68 channel or 34 channel logic analyzer module for the P6980 differential data and clock logic analyzer probe.

Table 6: Channel assignment for a P6980 differential clock and data logic analyzer probe to a 68 or 34 channel logic analyzer module

		68 Channel			
				34 Channel	
		Probe 2		Probe 1	
Pin number	Signal name	Head1	Head2	Head1	Head2
A1	D0+	A0:0+	D0:0+	C2:0+	A2:0+
A2	D0-	A0:0-	D0:0-	C2:0-	A2:0-
A3	GND	GND	GND	GND	GND
A4	D2+	A0:2+	D0:2+	C2:2+	A2:2+
A5	D2-	A0:2-	D0:2-	C2:2-	A2:2-
A6	GND	GND	GND	GND	GND
A7	D4+	A0:4+	D0:4+	C2:4+	A2:4+
A8	D4-	A0:4-	D0:4-	C2:4-	A2:4-
A9	GND	GND	GND	GND	GND
A10	D6+	A0:6+	D0:6+	C2:6+	A2:6+
A11	D6-	A0:6-	D0:6-	C2:6-	A2:6-
A12	GND	GND	GND	GND	GND
A13	NC	NC	ND	NC	NC
A14	NC	NC	ND	NC	NC
A15	GND	GND	GND	GND	GND
A16	D8+	A1:0+	D1:0+	C3:0+	A3:0+
A17	D8-	A1:0-	D1:0-	C3:0-	A3:0-
A18	GND	GND	GND	GND	GND
A19	D10+	A1:2+	D1:2+	C3:2+	A3:2+
A20	D10-	A1:2-	D1:2-	C3:2-	A3:2-
A21	GND	GND	GND	GND	GND
A22	D12+	A1:4+	D1:4+	C3:4+	A3:4+
A23	D12-	A1:4-	D1:4-	C3:4-	A3:4-
A24	GND	GND	GND	GND	GND
A25	D14+	A1:6+	D1:6+	C3:6+	A3:6+
A26	D14-	A1:6-	D1:6-	C3:6-	A3:6-
A27	GND	GND	GND	GND	GND

Table 6: Channel assignment for a P6980 differential clock and data logic analyzer probe to a 68 or 34 channel logic analyzer module (Cont.)

		68 Channel			
				34 Channel	
		Probe 2		Probe 1	
Pin number	Signal name	Head1	Head2	Head1	Head2
B1	GND	GND	GND	GND	GND
B2	D1-	A0:1-	D0:1-	C2:1-	A2:1-
B3	D1+	A0:1+	D0:1+	C2:1+	A2:1+
B4	GND	GND	GND	GND	GND
B5	D3-	A0:3-	D0:3-	C2:3-	A2:3-
B6	D3+	A0:3+	D0:3+	C2:3+	A2:3+
B7	GND	GND	GND	GND	GND
B8	D5-	A0:5-	D0:5-	C2:5-	A2:5-
B9	D5+	A0:5+	D0:5+	C2:5+	A2:5+
B10	GND	GND	GND	GND	GND
B11	D7-	A0:7-	D0:7-	C2:7-	A2:7-
B12	D7+	A0:7+	D0:7+	C2:7+	A2:7+
B13	GND	GND	GND	GND	GND
B14	CK-	CK1-	CK2-	CK3-	CK0-
B15	CK+	CK1+	CK2+	CK3+	CK0+
B16	GND	GND	GND	GND	GND
B17	D9-	A1:1-	D1:1-	C3:1-	A3:1-
B18	D9+	A1:1+	D1:1+	C3:1+	A3:1+
B19	GND	GND	GND	GND	GND
B20	D11-	A1:3-	D1:3-	C3:3-	A3:3-
B21	D11+	A1:3+	D1:3+	C3:3+	A3:3+
B22	GND	GND	GND	GND	GND
B23	D13-	A1:5-	D1:5-	C3:5-	A3:5-
B24	D13+	A1:5+	D1:5+	C3:5+	A3:5+
B25	GND	GND	GND	GND	GND
B26	D15-	A1:7-	D1:7-	C3:7-	A3:7-
B27	D15+	A1:7+	D1:7+	C3:7+	A3:7+

Specifications

Mechanical and Electrical Specifications

Table 7 lists the mechanical and electrical specifications for the P6960 and P6980 Probes. The electrical specifications apply when the probe is connected between a compatible logic analyzer and a target system.

Refer to the *Tektronix Logic Analyzer Family Product Specifications* document (Tektronix part number 071-1344-xx) available on the *Tektronix Logic Analyzer Family Product Documentation* CD or downloadable from the Tektronix Web site for a complete list of specifications, including overall system specifications.

Table 7: Mechanical and electrical specifications

Characteristic	P6960	P6980
Threshold accuracy	±(35 mV ±1% of setting)	±(35 mV ±1% of setting)
Input resistance	20 kΩ ±1%	20 kΩ ±1%
Input capacitance	0.5 pF (typical)	0.5 pF (typical)
Minimum digital signal swing	300 mV single-ended	150 mV differential each side
Maximum nondestructive input signal to probe	±15 V	±15 V
Delay from probe tip to module input connector	7.70 ns ±60 ps	7.70 ns ±60 ps
Probe length	1.8 m (6 ft)	1.8 m (6 ft)
Operating range	+5 V to -2.5 V	+5 V to -2.5 V

NOTE. *Because the length of the probes are electrically similar, they can be interchanged without problems.*

Table 8 shows the environmental specifications for the probes. The probes are designed to meet Tektronix standard 062-2847-00 class 5.

Table 8: Environmental specifications

Characteristic	P6960	P6980
Temperature		
Operating	0 °C to +50 °C	0 °C to +50 °C
Non-operating	-51 °C to +71 °C	-51 °C to +71 °C
Humidity	10 °C to 30 °C 95% relative humidity 30 °C to 40 °C 75% relative humidity 40 °C to 50 °C 45% relative humidity	10 °C to 30 °C 95% relative humidity 30 °C to 40 °C 75% relative humidity 40 °C to 50 °C 45% relative humidity
Altitude		
Operating	10,000 ft (3,048 m)	10,000 ft (3,048 m)
Non-operating	40,000 ft (12,192 m)	40,000 ft (12,192 m)
Electrostatic immunity	6 kV	6 kV

Maintenance

The P6960 and P6980 Probes do not require scheduled or periodic maintenance. Refer to the Functional Check section below to verify the basic functionality of the probes.

Probe Calibration

To confirm that the probes meet or exceed the performance requirements for published specifications with a compatible logic analyzer module, you must return the probes to your local Tektronix service center.

Functional Check

Connect the logic analyzer probes to a signal source, start an acquisition, and verify that the acquired data is displayed in either the listing or waveform windows.

Inspection and Cleaning

CAUTION. *To prevent damage during the probe connection process, do not touch the exposed edge of the interface clip. Do not drag the contacts against a hard edge or corner.*

To maintain a reliable electrical contact, keep the probes free of dirt, dust, and contaminants. Remove dirt and dust with a soft brush. Avoid brushing or rubbing the c-spring contacts. For more extensive cleaning, use only a damp cloth. Never use abrasive cleaners or organic solvents.

Service Strategy

The P6960 and P6980 Probes use replaceable c-spring cLGA clips. See page 38 for the replacement procedure. If a probe failure other than the cLGA clip occurs, return the entire probe to your Tektronix service center for repair.

Replacing the cLGA Clip

To replace the clip, do the following:

1. Gently pull one side of the clip away from the probe head, as shown in Figure 21, and then remove the entire clip.
2. Align the new clip with the probe head and gently snap it into place.
3. Test the probe to confirm that all channels are functional.

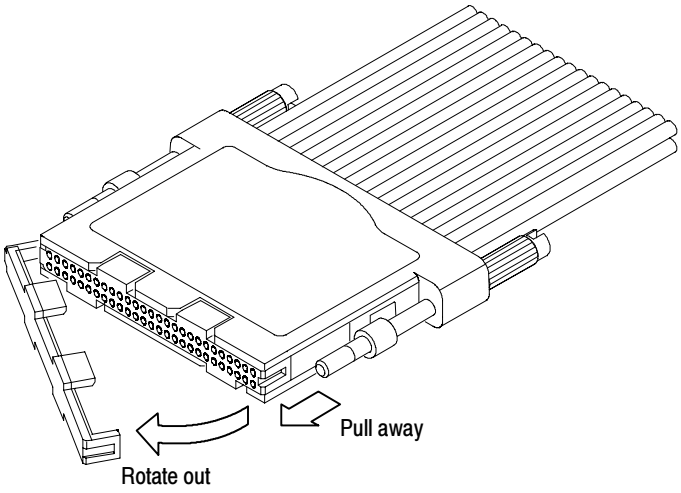

Figure 21: Replacing the cLGA clip

Legacy Probe and Attachment Support

- Nexus Technology, a Tektronix Partner, sells accessories that allow you to use the P6960 probe with legacy attachment connectors as well as utilize the P6960 probe footprint with select P68XX and P64XX probe products.
- Please contact Nexus Technology directly for more information.
- Contact Information:

  Nexus Technology
  Phone: 877-595-8116
  Fax: 877-595-8118

Repackaging Instructions

Use the original packaging, if possible, to return or store the probes. If the original packaging is not available, use a corrugated cardboard shipping carton. Add cushioning material to prevent the probes from moving inside the shipping container.

Enclose the following information when shipping the probe to a Tektronix Service Center.

- Owner's address
- Name and phone number of a contact person
- Type of probe
- Reason for return
- Full description of the service required

Replaceable Parts

This chapter contains a list of the replaceable components for the P6960 and P6980 Probes. Use this list to identify and order replacement parts.

Parts Ordering Information

Replacement parts are available through your local Tektronix field office or representative.

Changes to Tektronix products are sometimes made to accommodate improved components as they become available and to give you the benefit of the latest improvements. Therefore, when ordering parts, it is important to include the following information in your order.

- Part number
- Instrument type or model number
- Instrument serial number
- Instrument modification number, if applicable

If you order a part that has been replaced with a different or improved part, your local Tektronix field office or representative will contact you concerning any change in part number.

Using the Replaceable Parts List

Replaceable Parts

The P6960 and P6980 Probes contain only the elastomer as a replaceable part. If probe failure occurs, return the entire probe to your Tektronix service representative for repair.

Refer to the following list for replaceable items:

Parts list column descriptions

Column	Column name	Description
1	Figure & index number	Items in this section reference figure and index numbers to the exploded view illustrations that follow.
2	Tektronix part number	Use this part number when ordering replacement parts from Tektronix.
3 and 4	Serial number	Column three indicates the serial number at which the part was first effective. Column four indicates the serial number at which the part was discontinued. No entries indicates the part is good for all serial numbers.
5	Qty	This indicates the quantity of parts used.
6	Name & description	An item name is separated from the description by a colon (:). Because of space limitations, an item name may sometimes appear as incomplete. Use the U.S. Federal Catalog handbook H6-1 for further item name identification.
7	Mfr. code	This indicates the code of the actual manufacturer of the part.
8	Mfr. part number	This indicates the actual manufacturer's or vendor's part number.

Abbreviations

Abbreviations conform to American National Standard ANSI Y1.1–1972.

Mfr. Code to Manufacturer Cross Index

The table titled Manufacturers Cross Index shows codes, names, and addresses of manufacturers or vendors of components listed in the parts list.

Manufacturers cross index

Mfr. code	Manufacturer	Address	City, state, zip code
80009	TEKTRONIX INC	14150 SW KARL BRAUN DR PO BOX 500	BEAVERTON, OR 97077-0001

P6960 replaceable parts list

Figure & index number	Tektronix part number	Serial no. effective	Serial no. discont'd	Qty	Name & description	Mfr. code	Mfr. part number
22							
-1	010-6960-10			1	P6960 PROBE (INCLUDES SHEET OF LABELS AND PROBE LABELING INSTRUCTIONS)	80009	010-6960-10
					P6960 STANDARD ACCESSORIES		
-2	344-0610-00			1	CLIP,INTERFACE (CLGA); P6960/P6980 PROBE, SAFETY CONTROLLED	80009	344-0610-00
-3	200-4893-00			1	COVER,PROTECTIVE; BLACK VINYL (PLASTISOL) WITH STATIC-DISSIPATIVE ADDITIVE	80009	200-4893-00
	020-2539-00			1	KIT, RETENTION; P6960/P6980	80009	020-2539-00
	346-0300-00			1	STRAP,VELCRO;ONE WRAP,BLACK,0.500W X 8.00L,QTY 2 BAGGED & LABELED	80009	346-0300-00
	003-1890-00			1	TOOL,HAND; USED TO TIGHTEN PROBE HEAD TO DUT	80009	003-1890-00
	071-1539-XX			1	MANUAL,TECH; TRIFOLD,INSTALLATION/LABELING INSTRUCTIONS FOR P6960	80009	071-1539-XX
	071-1528-XX			1	MANUAL, TECH; INSTRUCTION, P6960/P6980 HIGH DENSITY LOGIC ANALYZER PROBE	80009	071-1528-XX
	335-1208-00			1	P6960 PROBE, SHEET OF LABELS	80009	335-1208-00

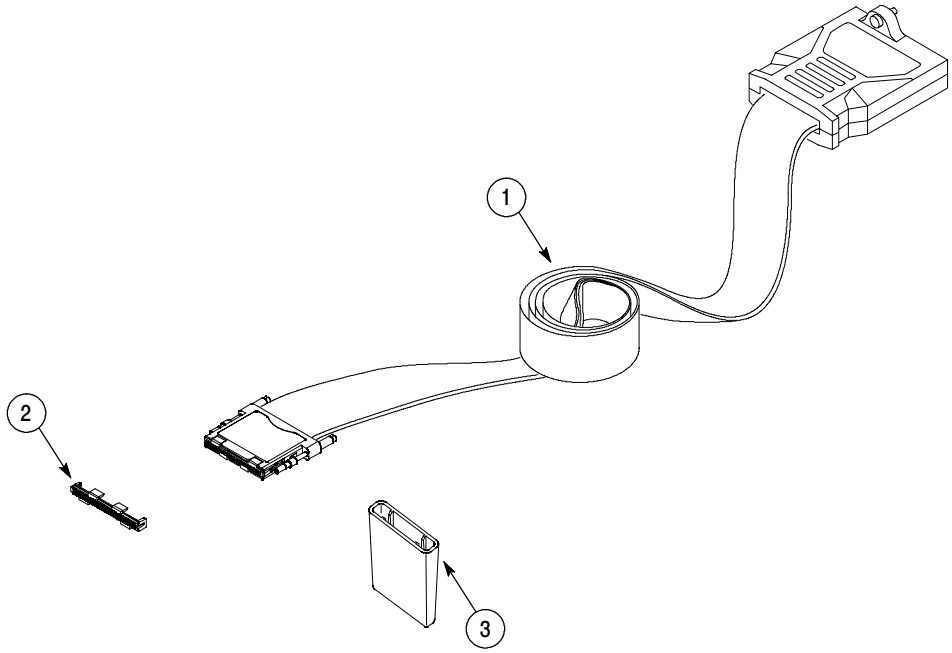

Figure 22: P6960 High-Density probe accessories

P6980 replaceable parts list

Figure & index number	Tektronix part number	Serial no. effective	Serial no. discont'd	Qty	Name & description	Mfr. code	Mfr. part number
-23							
-1	010-6980-10			1	P6980 PROBE SET (INCLUDES SHEET OF LABELS AND PROBE LABELING INSTRUCTIONS)	80009	010-6980-10
					P6980 STANDARD ACCESSORIES		
-2	344-0610-00			2	CLIP,INTERFACE (CLGA); P6960/P6980 PROBE, SAFETY CONTROLLED	80009	344-0610-00
-3	200-4893-00			2	COVER,PROTECTIVE; BLACK VINYL (PLASTISOL) WITH STATIC-DISSIPATIVE ADDITIVE	80009	200-4893-00
	020-2539-00			1	KIT, RETENTION; P6960/P6980	80009	020-2539-00
	346-0300-00			1	STRAP,VELCRO;ONE WRAP,BLACK,0.500W X 8.00L,QTY 2 BAGGED & LABELED	80009	346-0300-00
	003-1890-00			1	TOOL,HAND; USED TO TIGHTEN PROBE HEAD TO DUT	80009	003-1890-00
	071-1542-XX			1	MANUAL,TECH; TRIFOLD,INSTALLATION/LABELING INSTRUCTIONS FOR P6980	80009	071-1542-XX
	071-1528-XX			1	MANUAL, TECH; INSTRUCTION, P6960/P6980 HIGH DENSITY LOGIC ANALYZER PROBE	80009	071-1528-XX
	335-1209-00			1	P6980 PROBE, SHEET OF LABELS	80009	335-1209-00

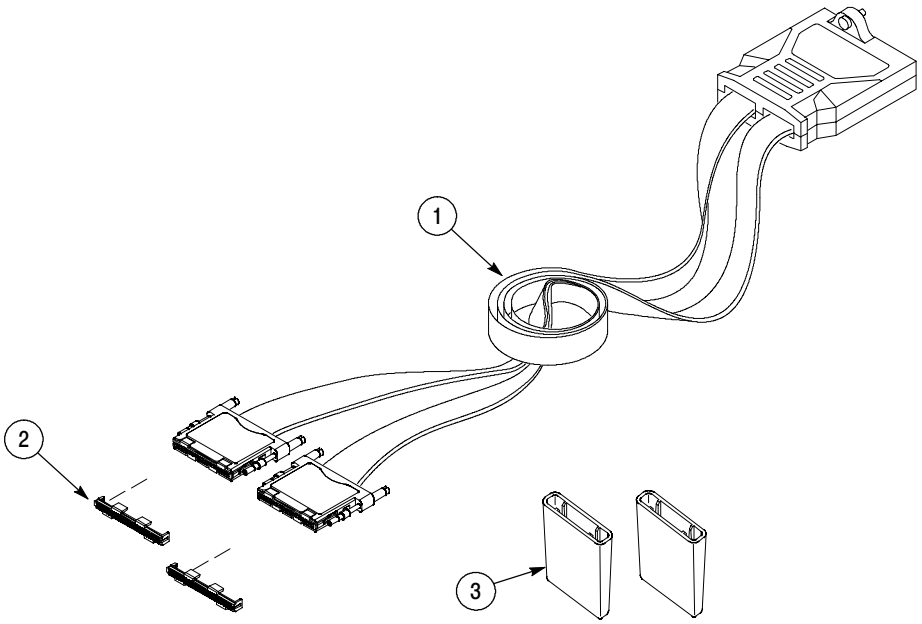

Figure 23: P6980 High-Density Differential probe accessories

P6960 and P6980 optional accessories

Figure & index number	Tektronix part number	Serial no. effective	Serial no. discont'd	Qty	Name & description	Mfr. code	Mfr. part number
24					**P6860 and P6880 OPTIONAL ACCESSORIES**		
-1	196-3494-00			1	P69xx FLYING LEADSET	80009	196-3494-00
-2	SMG50			1	ADAPTER KIT; BAG OF 20 KLIPCHIP ADAPTER (40 TOTAL)	80009	SMG50

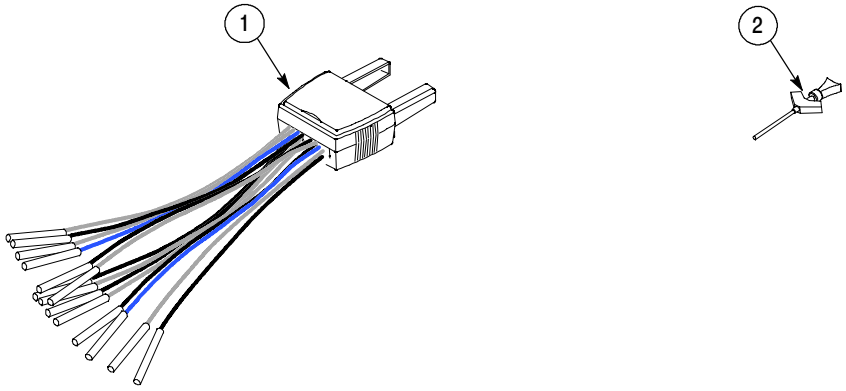

Figure 24: Optional accessories

Index

P

Q

R

S

T

U

W